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DERWENT-WEEK: 199841

TITLE: Evaluation of jig material used in semiconductor processing - conducts regular thermal processing of semiconductor wafer along with simultaneously held test piece of conformable geometry and made of currently used jig material

PATENT-ASSIGNEE: SUMITOMO METAL IND LTD[SUMQ]

PRIORITY-DATA: 1997JP-0001535 (January 8, 1997)

PATENT-FAMILY:

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ABSTRACTED-PUB-NO: JP 10199948A

BASIC-ABSTRACT: The evaluation of jig material as a possible contamination source of semiconductor wafers is essential in the various thermal processing operations employed. Between a stack of semiconductor wafers (12a,12b), is interposed a test piece (10) of conformable geometry at a typical spacing of 20mm.

The test piece and the jig used are of the same material and are held within a container (20) made either of quartz or silicon carbide. The container is nearly air-tight, with a characteristic gap (23) between the cover (21) and the container body (22) and undergoes the regular thermal processing within the furnace (14). Post-treatment inspection of the wafers establishes the relative suitability of various jig materials.

ADVANTAGE - Provides quick, inexpensive procedure of high sensitivity to screen

variety of jig materials. Helps to secure higher yields through reliable processing structures.

CHOSEN-DRAWING: Dwg.3/9

TITLE-TERMS:
EVALUATE JIG MATERIAL SEMICONDUCTOR PROCESS CONDUCTING REGULAR THERMAL PROCESS
SEMICONDUCTOR WAFER SIMULTANEOUS HELD TEST PIECE CONFORM GEOMETRY MADE CURRENT
JIG MATERIAL

DERWENT-CLASS: S03 U11

EPI-CODES: S03-E04A5; S03-E04F1; S03-E04F2; U11-C01B; U11-C02A; U11-F01B9; U11-F02A2;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1998-369455

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the method for evaluating simple about whether this material especially brings about contamination however to a semiconductor wafer on the occasion of the heat treatment process in the manufacture process of a semiconductor device, and appropriately about the method of evaluating the material used for the fixture for semiconductors.
[0002]
[Description of the Prior Art] Fixtures for semiconductors used for the manufacture process of a semiconductor device, such as a wafer boat and a process tube, are expected what does not cause contamination of the semiconductor wafer by the detrimental metal impurity in a semiconductor heat treatment process etc. In order to manufacture such a fixture for semiconductors, it is important to evaluate correctly the stain resistance to the semiconductor wafer of material used for a fixture. Conventionally, the following three methods mainly existed as this evaluation method.
[0003] The 1st method is the method of carrying out the fixed quantity of the metal impurity in the solution obtained by grinding fixture material and dissolving in an acid etc. by atomic absorption analysis, inductive-coupling type plasma analysis (ICP), etc.
[0004] The 2nd method is a method of actually producing fixtures for semiconductors, such as a process tube and a wafer boat, with the fixture material set as the object of evaluation, heat-treating a semiconductor wafer on the obtained fixture for semiconductors, and evaluating the pollution situation of a wafer.
[0005] The 3rd method is the method of carrying out the fixed quantity of the metal impurity by which heat-treated the body for metal uptakes covered, the matter, for example, the silicon nitride, with a diffusion coefficient smaller than a semiconductor of a metal impurity, with fixture material, and the uptake was carried out into covering of the body for metal uptakes (refer to JP,4-267327,A).
[0006] Although the kind and amount of a metal impurity which are contained in fixture material can be clarified by the 1st method, it cannot clarify about the actual degree of contamination which changes with the forms (for example, an oxide, carbide, etc.) of a metal impurity, and service conditions (temperature, atmosphere, etc.) of a fixture. By this method, fixture material cannot clarify whether it has how much influence on a semiconductor property in an actual heat treatment process.
[0007] It is necessary to actually make the target fixture as an experiment one by one by the 2nd method. The space for which a fixture also needs the heat treatment facility used for an examination receives restrictions. This method is not practical in respect of cost, time, and expedient nature.
[0008] By the 3rd method, although identification of a pollutant and a fixed quantity are possible like the 1st method, the influence on the semiconductor property in an actual heat treatment process does not become clear, either. As one example of this method, it heat-treats on both sides of the body for metal uptakes covered with silicon nitride etc. with fixture material, the metal impurity by which the uptake was carried out to covering is analyzed, and there is a method of evaluating the stain resistance of fixture material. However, it it heat-treats by contacting fixture material and the body for metal uptakes like this method, an oxygen cause stacking fault (Oxidation-Induced StackingFaults) ("OSF" is called hereafter) is induced, for example, and exact material evaluation becomes impossible. Moreover, since this method needs a special material called the body for metal uptakes, there is a problem also in the point of cost and evaluation time.
[0009]
[Problem(s) to be Solved by the Invention] The purpose of this invention is offering the method the material used for the fixture for semiconductors being evaluated simple and exactly, about the stain resistance to a semiconductor wafer.
[0010]
[Means for Solving the Problem] this invention is the method of evaluating the material used for the fixture for semiconductors. In the container which consists of material chosen from the group which consists of a quartz, silicon carbide, silicon, and those combination, and has an air hole The process which the test piece and semiconductor wafer which consist of material used for the fixture for semiconductors are made to counter so that a mutual distance may be set to 20mm or less, without making it contact mutually, and holds them, It has the process which heats a test piece and a semiconductor wafer in a heat treating furnace in the state where it held in the container, and the process which measures the property of a semiconductor wafer after a heating process. The size of the air hole of the container which holds a test piece and a semiconductor wafer is a size which is the grade which can perform aeration, suppressing contamination of the semiconductor wafer from the atmosphere besides a heat treating furnace and this container in a heating process. The stain resistance to the semiconductor wafer by the material used for the

fixture for semiconductors can be evaluated by measuring the property of the semiconductor wafer heated with the test piece.
[0011] The container which holds a test piece and a semiconductor wafer shall form the space for holding a test piece and a semiconductor wafer according to one pair of bases which counter, and the side inserted into them. In this case, as for the effective-area product in the air hole prepared in a container, it is desirable to be referred to as one of 1 / 20 - 1/10 of area. [of one pair of bases]
[0012]
[Embodiments of the Invention] this invention is applied to evaluation of the material which constitutes fixtures for semiconductors used for a semiconductor device manufacture process, such as a wafer boat and a process tube. Using the fixture material of the configuration of having been suitable for simple and exact evaluation, and a size, this invention can lessen restrictions of a test facility and can make the burden of costs and time light. For example, it is more practical to make almost the same as the semiconductor wafer held in [both] a container the configuration and size of fixture material which are held in a container for evaluation, and it is more desirable.
[0013] In this invention, the test piece which consists of a charge of fixture material fabricated by a suitable configuration and a suitable size, and a semiconductor wafer are held in the container of half-sealing which consists of material chosen from the group which consists of a quartz, silicon carbide, silicon, and those combination. This container plays the role which protects the test piece and semiconductor wafer which are held in inside from the influence of a heat treating furnace and heating atmosphere in a next heating process. Moreover, a container has a crevice between the sizes which are the grades which can perform aeration, suppressing contamination of a heat treating furnace and the semiconductor wafer from the atmosphere besides a container in a heating process. By this crevice, circulation between the atmosphere in a container and the atmosphere outside a container can be performed gradually, and influence on the test piece and semiconductor wafer from the container itself and the atmosphere in a container can be made small. A container encloses and protects a test piece and a semiconductor wafer, and the environment for exact evaluation is brought about so that the influence from a test piece to a semiconductor wafer may not be blocked by influence from other factors. Since what does not have influence of contamination on a test piece and a semiconductor wafer as much as possible in a heating process is desirable as for a container, a quartz, silicon carbide, silicon, or those combination are chosen as the material. There is material (for example, carbon material) covered with the thing which carried out the CVD coat of the silicon carbide to the nature composite material of silicon carbide which consists of quartz glass, the sintered compact of silicon carbide, silicon carbide, and silicon, silicon, and silicon carbide as a more desirable material, and the CVD coat film of silicon carbide. In the material which constitutes a container, the concentration of each metal impurity has desirable 1 ppm or less. A container may constitute the whole from one kind of material, and may constitute it from a portion which consists of a different material. Moreover, on the base material which consists of a specific material, other materials may be coated and a container may be formed.
[0014] The test piece and semiconductor wafer which were held in the container are heated in a heat treating furnace. Drawing 1 shows one example of this invention, and shows signs that it heats in a heat treating furnace where a test piece and a semiconductor wafer are held in a container. In the heat treating furnace 14, the half-airtight container 20 which holds the test piece 10 and the semiconductor wafers 12a and 12b which consist of a charge of fixture material is laid. Let a test piece 10 be the almost same configuration and size as the semiconductor wafers 12a and 12b. Thereby, structure of the half-airtight container 20 can be simplified and dispersion in the evaluation obtained can also be decreased. It heat-treats by holding in the half-airtight container 20 in the state where the test piece 10 was made to counter the semiconductor wafers 12a and 12b. the temperature in a furnace 14 is raised to predetermined temperature at a heater 15, and required in heat treatment, -- time maintenance is carried out O2 [moreover,] used for a semiconductor device manufacture process on the occasion of heat treatment etc. -- predetermined gas -- introduction -- it introduces in a furnace 14 through a hole 16, and a predetermined atmosphere is brought about
[0015] As shown in drawing 1 , the half-airtight container 20 consists of wrap lids 21 in it with the base material 22 which holds a test piece 10 and the semiconductor wafers 12a and 12b. The shelf for supporting a test piece and a wafer is formed in the base material 22, and where a test piece and a semiconductor wafer are detached in a predetermined distance, it can hold now to parallel mostly. In a base material 22, although at least two shelves are formed so that at least one test piece and a semiconductor wafer can be held, the number can be set up if needed or more by two. The base material which has a suitable number of shelves according to the number of test pieces to evaluate can be used. Although a test piece and a semiconductor wafer are held in the state where it was surrounded by the lid 21 and base material 22 which constitute a container 20, the crevice 23 is formed between the base material 22 and the lid 21, and the interior of a container is connected with the container exterior by the air hole which consists of crevices 23. As a crevice 23 makes influence of contamination by the influence of contamination from the heat treating furnace itself, and introductory gas, and influence of contamination from a half-airtight container as small as possible, let it be a suitable size, so that it may mention later.
[0016] More detailed structure is shown about one example of the base material which constitutes a half-airtight container in drawing 2 and drawing 3 , and a lid. The base material 22 shown in drawing 2 is a box-like form whose end is opening. Not a perfect barrel but the part lacks the side attachment wall of a base material 22. The shelves 22a, 22b, and 22c formed in the side attachment wall convex support a test piece and a semiconductor wafer. The lid 21 shown in drawing 3 is larger than a base material 22 a little, and when this is put on a base material 22, it has come to be able to do a crevice so that an edge may be the box-like form which is opening and can cover a base material 22 on the other hand. Drawing 4 shows signs that a crevice is made. If a test piece and a semiconductor wafer are laid in the shelf of a base material 22 and a lid 21 is put, a state required for heat treatment will be done.

[0017] As shown in drawing 1 , a test piece 10 and the semiconductor wafers 12a and 12b are held in a container 20 so that it may not contact mutually. The interval of the test piece 10 and the semiconductor wafers 12a or 12b which are countered and held is set as 20mm or less, and is preferably set as the range of 0.3mm - 10mm. When this interval exceeds 20mm, about a semiconductor wafer, compared with the influence from a test piece, the influence from the atmosphere in a container becomes large relatively, and evaluation exact about the stain resistance to the semiconductor wafer of a test piece becomes impossible. In addition, if an interval is less than 0.3mm, a test piece and a semiconductor wafer will become easy to contact. When these contact, evaluation exact for OSF generated to a semiconductor wafer so that it may mention later becomes impossible. Moreover, as for the touch area with the base material 22 of the half-airtight container 20, a test piece, and a semiconductor wafer, it is desirable to make it as small as possible in the range which is stabilized and can support these. If a touch area becomes large, especially in a semiconductor wafer, it will become easy to generate a defect. When a defect generates mostly, there is a possibility that the correctness of evaluation may be spoiled. More exact evaluation can be obtained by making these touch areas as small as possible.

[0018] In the half-airtight container 20, the crevice 23 between a base material 22 and a lid 21 is set as a suitable size so that the influence of contamination from a heat treating furnace and heating atmosphere can be suppressed in a heating process. Drawing 4 shows the cross section of the half-airtight container 20 which comes to cover a base material 22 a lid 21. The crevice 23 is formed between the base material 22 and the lid 21. A crevice 23 forms the air hole which connects the inside of a container, and outside. As for the effective-area product of this air hole, i.e., the area of a crevice 23, it is desirable that it is in the range of 1 / 20 - 1/10 of the area of bottom 22e of a base material 22. If the area of a crevice is smaller than 1/20 of areas of base, the influence of the atmosphere in the half-airtight container 20 will become large relatively. That is, it becomes difficult to control the atmosphere in a half-airtight container in the atmosphere for the purpose of an examination. If the area of a crevice is larger than 1/10 of areas of base, the influence of the contamination from a heat treating furnace and the contamination from introductory gas will become large. The correctness of evaluation will come to be spoiled if these influences become large too much. this invention holds a test piece and a semiconductor wafer in the container which has a crevice between suitable sizes, avoids the influence mentioned above as much as possible, and offers the method of measuring the influence to the semiconductor wafer of fixture material certainly.

[0019] As for heat treatment conditions, such as temperature, time, and atmosphere, it is common to double with the conditions for which a fixture is used in the manufacture process of a semiconductor device. However, even if it shortens heat treatment time or carries out by raising temperature if needed, it does not interfere.

[0020] The stain resistance to the semiconductor wafer by the influence to a semiconductor wafer, i.e., the fixture material, of a test piece can be evaluated by measuring the property of a semiconductor wafer after heat treatment. The method usually used for material evaluation of a silicon wafer etc. is applicable to the method of measuring the property of a semiconductor wafer. As a method of measuring the property of a semiconductor wafer, a life-time measuring method, an OSF measuring method, a scaling film analysis method, etc. can be used. A life-time measuring method is the method of measuring the half-life of the carrier generated when it is also called microwave vibration decay method and a semiconductor wafer is excited with light etc. Since a half-life becomes short by contamination of a heavy-metal impurity, evaluation of the degree of contamination of a wafer can be performed comparatively simply by measuring this. If a life time is large, a test piece means that purity is high and it is suitable with a fixture small [the degree of the contamination to a semiconductor wafer from a test piece] therefore. OSF is the stacking fault generated during oxidation treatment, and is generated by heavy metal or the mechanical blemish. By the OSF measuring method, the wafer for monitors is **********ed and the number of pits resulting from OSF is measured using a metaloscope. When there is little OSF measured in the semiconductor wafer, the degree of the contamination to a wafer from a test piece is small, therefore fixture material has high purity, and since a fixture is constituted, a desirable thing is meant. When a scaling film analysis method oxidizes in an oxidizing atmosphere, it carries out the fixed quantity of the impurity in the scaling film generated to a semiconductor wafer, and it clarifies a pollution source. By this method, the fixed quantity of the impurity is carried out, for example by atomic absorption analysis. Thus, by measuring the property of the semiconductor wafer heat-treated with the test piece, the stain resistance to the semiconductor wafer of fixture material can be evaluated, and it can grasp simple and exactly whether the material is suitable for the fixture for semiconductors.

[0021]

[Example]

It evaluated about the fixture material A, B, and C for semiconductors which consists of three kinds of silicon carbide sintered compacts which have the purity shown in example 1 table 1, respectively. It considered as the wafer for monitors for material evaluation of the 4 inch silicon wafer usually used for manufacture of a semiconductor device. What was prepared about three kinds of fixture material in the respectively same configuration and respectively same size as a 4 inch silicon wafer was used as a test piece. As the test piece and monitor wafer which consist of each fixture material were shown in the half-airtight container made from a quartz which consists of a lid as shown in a base material as shown in drawing 2 , and drawing 3 at drawing 1 , it held in the half-airtight container. That is, each test piece was laid between two wafers for monitors which counter. The interval of the wafer for monitors and the piece of fixture material testing was 5mm. The area of the crevice made when a lid is put on a base material was 1/15 of the area of base of a base material. Where a test piece and the wafer for monitors are held in a half-airtight container, as shown in drawing 1 , it sets to a heat treating furnace, and it is dryness O2. 1200 degrees C and heat treatment of 2 hours were performed under atmosphere.

[0022] The wafer for monitors was taken out after heat treatment, and the property of a wafer was measured. According to the usual method, it measured about the metal impurity in the life time (LT) of the field which had countered the test piece of the

wafer for monitors, the OSF number, and an oxide film. The life time was measured by Leo Research Institute LTA-33A. The OSF number was measured with the metaloscope as mentioned above. The metal impurity in an oxide film measured by frame loess atomic absorption analysis. The result of measurement is shown in Table 2. There is no conflict between the measured value of the metal impurity in a life time, the OSF number, and an oxide film, and accurate evaluation was completed about each material by these.

[0023] Drawing 5 shows the distribution of the life time on the wafer for monitors heat-treated with the test piece of Material A. Drawing 6 shows the distribution of the life lime on the wafer for monitors heated with the test piece of Material B. All over drawing, it is shown in accordance with the relation of the size of a black rectangular head and the length of a half-life which were written in. A life time means a ********, so that the black rectangular head in drawing is large. When these are compared, it turns out that the life time about the wafer for monitors about the material B with many metal impurities is short. It is proved further that this has a proper this invention as an appraisal method of material. Moreover, the difference of a life time shown in drawing 5 and drawing 6 to the analysis values of Material A and Material B differing slightly by the analysis result which shows in Table 1 what should be observed is a remarkable thing. That is, it turns out that it is difficult to evaluate exactly the superiority or inferiority of the stain resistance to the wafer only by analyzing the metal impurity in material.

[0024] On both sides of the test piece which consists of example of comparison 1 each material, it laid in two wafers for monitors at the same shelf of an airtight container. That is, the wafer for monitors and the test piece were contacted mutually, and were held in the container. Except it, it processed on the same conditions as an example 1, and measured about the property of the wafer for monitors. The obtained result is shown in Table 2. About the life time, although the same result as an example 1 was obtained, the evaluation about Material A and Material B was reversed [number / OSF]. Moreover, the value about the material C about the OSF number was unusually large. These results show that it is unsuitable in the evaluation method to contact the wafer for monitors and a test piece.

[0025] Except having used the half-airtight container which consists of an example 2 silicon-carbide sintered compact, it processed under the same conditions as an example 1, and measured about the property of the wafer for monitors. The obtained result is shown in Table 2. The result shows the same inclination as an example 1, and was understood that the evaluation method of following this invention is proper.

[0026] The cassette boat used for heat treatment of a silicon wafer with each material of the silicon carbide sintered compact which is a candidate for example of comparison 2 evaluation was produced. It lays in the cassette boat which produced the 4 inch silicon wafer, it sets to a heat treating furnace, and is dryness O2. 1200 degrees C and heat treatment of 2 hours were performed among atmosphere. Drawing 7 shows signs that a silicon wafer 72 is laid on the cassette boat 70. Thus, about the silicon wafer which actually heat-treated on the cassette boat, the metal impurity in a life time, the OSF number, and an oxide film was measured like the example 1. The obtained result is shown in Table 2. Moreover, the distribution of the life time in the heat-treated silicon wafer is shown in drawing 8 . In the distribution shown in drawing 8 , as for the portion (portion under drawing) which touches the cassette boat in a wafer, the life time is short unusually. However, this is based on local contamination, and the influence of the average on the whole life-time value is comparatively small as the result of Table 2 shows. Therefore, it turns out that it is dangerous.

[0027] It processed on the same conditions as an example 1 except having used for the half-airtight container the base material in which a shelf from which the distance of example of comparison 3 test piece and the wafer for monitors is set to 25mm was formed. After heat-treating the test piece of Material A with the wafer for monitors within a half-airtight container, the life-time distribution on a wafer was measured like the example 1. The result is shown in drawing 9 . As shown in drawing, the life time is short unusually and it was thought near the periphery section of the wafer for monitors that this portion was contamination by the atmosphere inside a half-airtight container. Therefore, when the distance between a test piece and the wafer for monitors was too large, the bird clapper found exact evaluation difficult.

[0028]

[Table 1]

特性 / 試料	基材純度(ppm) Fe	Ni	Cu	Cr	Al
領域 材料 A	<0.5	<1	<0.2	<0.5	2
〃 B	<0.5	<1	<0.2	<0.5	<1
〃 C	3	<1	<0.2	<0.5	<1

Tr : 0.01 ppm以下

[0029]

[Table 2]

特性 / 試料	LT (μS)	OSF (個/cm²)	検出限界(×10¹⁰atom/cm²) Fe	Ni	Cu	Zn	Al
実施例1 材料A	356	2	2.0	<3.6	5.1	0.4	<2.2
〃 B	72	15	21	<3.6	4.4	0.4	<2.2
〃 C	5.1	80	105	195	5.2	4.1	<2.2
比較例1 材料A	323	25	2.3	<3.6	5.8	2.1	<2.2
〃 B	57	12	23	<3.6	3.5	0.7	<2.2
〃 C	4.6	2000	111	242	6.4	2.6	<2.2
実施例2 材料A	347	6	2.2	<3.6	3.5	0.6	<2.2
〃 B	68	24	26	<3.6	6.3	1.1	<2.2
〃 C	4.9	103	102	126	7.9	5.7	<2.2
比較例2 材料A	540	1	<1.2	<3.6	4.5	0.6	<2.2
〃 B	412	5	<1.2	<3.6	5.1	0.9	<2.2
〃 C	305	20	2.0	59	6.7	0.5	<2.2

[0030]
[Effect of the Invention] While the metal impurity emitted from fixture material during elevated-temperature heat treatment is detectable to easy and high sensitivity as mentioned above according to this invention, influence of the semiconductor property on fixture material can be clarified. As mentioned above, according to this invention, the impurity in fixture material can evaluate the influence which it has on a wafer property with a sufficient precision. this invention does not need special metal uptake material or the fixture itself which is used for the conventional method, but can be evaluated simple and quickly about more kinds of fixture material. In this point, this invention is excellent in respect of [conventional method] cost and time. this invention estimates fixture material, and if a more suitable material is found out and a fixture is manufactured, the fixture for semiconductors greatly contributed to the manufacture yield of a semiconductor device and improvement in reliability can be offered.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] It is the evaluation method of the fixture material for semiconductors which the size of the air hole of the aforementioned container is the size which is the grade which can perform aeration, suppressing contamination of the aforementioned semiconductor wafer from the atmosphere besides the aforementioned heat treating furnace and the aforementioned container in the aforementioned heating process, and is characterized by having the following by to evaluate the stain resistance to the semiconductor wafer by the material used for the aforementioned fixture for semiconductors by measuring the property of the aforementioned semiconductor wafer. The process which the test piece and the semiconductor wafer which consist of material used for the aforementioned fixture for semiconductors are made to counter so that a mutual distance may be set to 20mm or less, without making it contact mutually, and holds them in the container which is the method of evaluating the material used for the fixture for semiconductors, consists of material chosen from the group which consists of a quartz, silicon carbide, silicon, and those combination, and has an air hole. The process which heats the aforementioned test piece and the aforementioned semiconductor wafer in a heat treating furnace in the state where it held in the aforementioned container. The process which measures the property of the aforementioned semiconductor wafer after the aforementioned heating process.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] this invention is the method of evaluating the material used for the fixture for semiconductors. In the container which consists of material chosen from the group which consists of a quartz, silicon carbide, silicon, and those combination, and has an air hole The process which the test piece and semiconductor wafer which consist of material used for the fixture for semiconductors are made to counter so that a mutual distance may be set to 20mm or less, without making it contact mutually, and holds them, It has the process which heats a test piece and a semiconductor wafer in a heat treating furnace in the state where it held in the container, and the process which measures the property of a semiconductor wafer after a heating process. The size of the air hole of the container which holds a test piece and a semiconductor wafer is a size which is the grade which can perform aeration, suppressing contamination of the semiconductor wafer from the atmosphere besides a heat treating furnace and this container in a heating process. The stain resistance to the semiconductor wafer by the material used for the fixture for semiconductors can be evaluated by measuring the property of the semiconductor wafer heated with the test piece.
[0011] The container which holds a test piece and a semiconductor wafer shall form the space for holding a test piece and a semiconductor wafer according to one pair of bases which counter, and the side inserted into them. In this case, as for the effective-area product in the air hole prepared in a container, it is desirable to be referred to as one of 1 / 20 - 1/10 of area. [of one pair of bases]
[0012]
[Embodiments of the Invention] this invention is applied to evaluation of the material which constitutes fixtures for semiconductors used for a semiconductor device manufacture process, such as a wafer boat and a process tube. Using the fixture material of the configuration of having been suitable for simple and exact evaluation, and a size, this invention can lessen restrictions of a test facility and can make the burden of costs and time light. For example, it is more practical to make almost the same as the semiconductor wafer held in [both] a container the configuration and size of fixture material which are held in a container for evaluation, and it is more desirable.
[0013] In this invention, the test piece which consists of a charge of fixture material fabricated by a suitable configuration and a suitable size, and a semiconductor wafer are held in the container of half-sealing which consists of material chosen from the group which consists of a quartz, silicon carbide, silicon, and those combination. This container plays the role which protects the test piece and semiconductor wafer which are held in inside from the influence of a heat treating furnace and heating atmosphere in a next heating process. Moreover, a container has a crevice between the sizes which are the grades which can perform aeration, suppressing contamination of a heat treating furnace and the semiconductor wafer from the atmosphere besides a container in a heating process. By this crevice, circulation between the atmosphere in a container and the atmosphere outside a container can be performed gradually, and influence on the test piece and semiconductor wafer from the container itself and the atmosphere in a container can be made small. A container encloses and protects a test piece and a semiconductor wafer, and the environment for exact evaluation is brought about so that the influence from a test piece to a semiconductor wafer may not be blocked by influence from other factors. Since what does not have influence of contamination on a test piece and a semiconductor wafer as much as possible in a heating process is desirable as for a container, a quartz, silicon carbide, silicon, or those combination are chosen as the material. There is material (for example, carbon material) covered with the thing which carried out the CVD coat of the silicon carbide to the nature composite material of silicon carbide which consists of quartz glass, the sintered compact of silicon carbide, silicon carbide, and silicon, silicon, and silicon carbide as a more desirable material, and the CVD coat film of silicon carbide. In the material which constitutes a container, the concentration of each metal impurity has desirable 1 ppm or less. A container may constitute the whole from one kind of material, and may constitute it from a portion which consists of a different material. Moreover, on the base material which consists of a specific material, other materials may be coated and a container may be formed.
[0014] The test piece and semiconductor wafer which were held in the container are heated in a heat treating furnace. Drawing 1 shows one example of this invention, and shows signs that it heats in a heat treating furnace where a test piece and a semiconductor wafer are held in a container. In the heat treating furnace 14, the half-airtight container 20 which holds the test piece 10 and the semiconductor wafers 12a and 12b which consist of a charge of fixture material is laid. Let a test piece 10 be the almost same configuration and size as the semiconductor wafers 12a and 12b. Thereby, structure of the half-airtight container 20 can be simplified and dispersion in the evaluation obtained can also be decreased. It heat-treats by holding in the half-airtight container 20 in the state where the test piece 10 was made to counter the semiconductor wafers 12a and 12b. the temperature in a furnace 14 is raised to predetermined temperature at a heater 15, and required in heat treatment, -- time maintenance is carried out O2 [moreover,] used for a semiconductor device manufacture process on the occasion of heat treatment etc. --

predetermined gas -- introduction -- it introduces in a furnace 14 through a hole 16, and a predetermined atmosphere is brought about

[0015] As shown in drawing 1 , the half-airtight container 20 consists of wrap lids 21 in it with the base material 22 which holds a test piece 10 and the semiconductor wafers 12a and 12b. The shelf for supporting a test piece and a wafer is formed in the base material 22, and where a test piece and a semiconductor wafer are detached in a predetermined distance, it can hold now to parallel mostly. In a base material 22, although at least two shelves are formed so that at least one test piece and a semiconductor wafer can be held, the number can be set up if needed or more by two. The base material which has a suitable number of shelves according to the number of test pieces to evaluate can be used. Although a test piece and a semiconductor wafer are held in the state where it was surrounded by the lid 21 and base material 22 which constitute a container 20, the crevice 23 is formed between the base material 22 and the lid 21, and the interior of a container is connected with the container exterior by the air hole which consists of crevices 23. As a crevice 23 makes influence of contamination by the influence of contamination from the heat treating furnace itself, and introductory gas, and influence of contamination from a half-airtight container as small as possible, let it be a suitable size, so that it may mention later.

[0016] More detailed structure is shown about one example of the base material which constitutes a half-airtight container in drawing 2 and drawing 3 , and a lid. The base material 22 shown in drawing 2 is a box-like form whose end is opening. Not a perfect barrel but the part lacks the side attachment wall of a base material 22. The shelves 22a, 22b, and 22c formed in the side attachment wall convex support a test piece and a semiconductor wafer. The lid 21 shown in drawing 3 is larger than a base material 22 a little, and when this is put on a base material 22, it has come to be able to do a crevice so that an edge may be the box-like form which is opening and can cover a base material 22 on the other hand. Drawing 4 shows signs that a crevice is made. If a test piece and a semiconductor wafer are laid in the shelf of a base material 22 and a lid 21 is put, a state required for heat treatment will be done.

[0017] As shown in drawing 1 , a test piece 10 and the semiconductor wafers 12a and 12b are held in a container 20 so that it may not contact mutually. The interval of the test piece 10 and the semiconductor wafers 12a or 12b which are countered and held is set as 20mm or less, and is preferably set as the range of 0.3mm - 10mm. When this interval exceeds 20mm, about a semiconductor wafer, compared with the influence from a test piece, the influence from the atmosphere in a container becomes large relatively, and evaluation exact about the stain resistance to the semiconductor wafer of a test piece becomes impossible. In addition, if an interval is less than 0.3mm, a test piece and a semiconductor wafer will become easy to contact. When these contact, evaluation exact for OSF generated to a semiconductor wafer so that it may mention later becomes impossible. Moreover, as for the touch area with the base material 22 of the half-airtight container 20, a test piece, and a semiconductor wafer, it is desirable to make it as small as possible in the range which is stabilized and can support these. If a touch area becomes large, especially in a semiconductor wafer, it will become easy to generate a defect. When a defect generates mostly, there is a possibility that the accuracy of evaluation may be spoiled. More exact evaluation can be obtained by making these touch areas as small as possible.

[0018] In the half-airtight container 20, the crevice 23 between a base material 22 and a lid 21 is set as a suitable size so that the influence of contamination from a heat treating furnace and heating atmosphere can be suppressed in a heating process. Drawing 4 shows the cross section of the half-airtight container 20 which comes to cover a base material 22 a lid 21. The crevice 23 is formed between the base material 22 and the lid 21. A crevice 23 forms the air hole which connects the inside of a container, and outside. As for the effective-area product of this air hole, i.e., the area of a crevice 23, it is desirable that it is in the range of 1 / 20 - 1/10 of the area of bottom 22e of a base material 22. If the area of a crevice is smaller than 1/20 of areas of base, the influence of the atmosphere in the half-airtight container 20 will become large relatively. That is, it becomes difficult to control the atmosphere in a half-airtight container in the atmosphere for the purpose of an examination. If the area of a crevice is larger than 1/10 of areas of base, the influence of the contamination from a heat treating furnace and the contamination from introductory gas will become large. The accuracy of evaluation will come to be spoiled if these influences become large too much. this invention holds a test piece and a semiconductor wafer in the container which has a crevice between suitable sizes, avoids the influence mentioned above as much as possible, and offers the method of measuring the influence to the semiconductor wafer of fixture material certainly.

[0019] As for heat treatment conditions, such as temperature, time, and atmosphere, it is common to double with the conditions for which a fixture is used in the manufacture process of a semiconductor device. However, even if it shortens heat treatment time or carries out by raising temperature if needed, it does not interfere.

[0020] The stain resistance to the semiconductor wafer by the influence to a semiconductor wafer, i.e., the fixture material, of a test piece can be evaluated by measuring the property of a semiconductor wafer after heat treatment. The method usually used for material evaluation of a silicon wafer etc. is applicable to the method of measuring the property of a semiconductor wafer. As a method of measuring the property of a semiconductor wafer, a life-time measuring method, an OSF measuring method, a scaling film analysis method, etc. can be used. A life-time measuring method is the method of measuring the half-life of the carrier generated when it is also called microwave vibration decay method and a semiconductor wafer is excited with light etc. Since a half-life becomes short by contamination of a heavy-metal impurity, evaluation of the degree of contamination of a wafer can be performed comparatively simply by measuring this. If a life time is large, a test piece means that purity is high and it is suitable with a fixture small [the degree of the contamination to a semiconductor wafer from a test piece] therefore. OSF is the stacking fault generated during oxidation treatment, and is generated by heavy metal or the mechanical blemish. By the OSF measuring method, the wafer for monitors is **********ed and the number of pits resulting from OSF is measured using a metaloscope. When there is little OSF measured in the semiconductor wafer, the degree of the contamination to a wafer from a test piece is

small, therefore fixture material has high purity, and since a fixture is constituted, a desirable thing is meant. When a scaling film analysis method oxidizes in an oxidizing atmosphere, it carries out the fixed quantity of the impurity in the scaling film generated to a semiconductor wafer, and it clarifies a pollution source. By this method, the fixed quantity of the impurity is carried out, for example by atomic absorption analysis. Thus, by measuring the property of the semiconductor wafer heat-treated with the test piece, the stain resistance to the semiconductor wafer of fixture material can be evaluated, and it can grasp simple and exactly whether the material is suitable for the fixture for semiconductors.

[Translation done.]

* NOTICES *

PRIOR ART

[Description of the Prior Art] Fixtures for semiconductors used for the manufacture process of a semiconductor device, such as a wafer boat and a process tube, are expected what does not cause contamination of the semiconductor wafer by the detrimental metal impurity in a semiconductor heat treatment process etc. In order to manufacture such a fixture for semiconductors, it is important to evaluate correctly the stain resistance to the semiconductor wafer of material used for a fixture. Conventionally, the following three methods mainly existed as this evaluation method.

[0003] The 1st method is the method of carrying out the fixed quantity of the metal impurity in the solution obtained by grinding fixture material and dissolving in an acid etc. by atomic absorption analysis, inductive-coupling type plasma analysis (ICP), etc.

[0004] The 2nd method is a method of actually producing fixtures for semiconductors, such as a process tube and a wafer boat, with the fixture material set as the object of evaluation, heat-treating a semiconductor wafer on the obtained fixture for semiconductors, and evaluating the pollution situation of a wafer.

[0005] The 3rd method is the method of carrying out the fixed quantity of the metal impurity by which heat-treated the body for metal uptakes covered, the matter, for example, the silicon nitride, with a diffusion coefficient smaller than a semiconductor of a metal impurity, with fixture material, and the uptake was carried out into covering of the body for metal uptakes (refer to JP,4-267327,A).

[0006] Although the kind and amount of a metal impurity which are contained in fixture material can be clarified by the 1st method, it cannot clarify about the actual degree of contamination which changes with the forms (for example, an oxide, carbide, etc.) of a metal impurity, and service conditions (temperature, atmosphere, etc.) of a fixture. By this method, fixture material cannot clarify whether it has how much influence on a semiconductor property in an actual heat treatment process.

[0007] It is necessary to actually make the target fixture as an experiment one by one by the 2nd method. The space for which a fixture also needs the heat treatment facility used for an examination receives restrictions. This method is not practical in respect of cost, time, and expedient nature.

[0008] By the 3rd method, although identification of a pollutant and a fixed quantity are possible like the 1st method, the influence on the semiconductor property in an actual heat treatment process does not become clear, either. As one example of this method, it heat-treats on both sides of the body for metal uptakes covered with silicon nitride etc. with fixture material, the metal impurity by which the uptake was carried out to covering is analyzed, and there is a method of evaluating the stain resistance of fixture material. However, it it heat-treats by contacting fixture material and the body for metal uptakes like this method, an oxygen cause stacking fault (Oxidation-Induced StackingFaults) ("OSF" is called hereafter) is induced, for example, and exact material evaluation becomes impossible. Moreover, since this method needs a special material called the body for metal uptakes, there is a problem also in the point of cost and evaluation time.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the method for evaluating simple about whether this material especially brings about contamination however to a semiconductor wafer on the occasion of the heat treatment process in the manufacture process of a semiconductor device, and appropriately about the method of evaluating the material used for the fixture for semiconductors.

[Translation done.]

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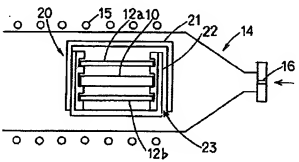
(54)【発明の名称】　半導体用治具材料の評価方法

(57)【要約】
【課題】　半導体装置の製造プロセスに用いられる治具を構成する材料が熱処理工程において半導体ウェハをどれだけ汚染するかについて簡便かつ的確に評価することのできる方法を提供する。
【解決手段】　石英または炭化ケイ素からなる半密閉容器２０内に、評価すべき半導体用治具の材料からなる試験片１０と半導体ウェハ１２ａ、１２ｂとを互いに接触させずにかつ互いの距離が２０ｍｍ以下となるように対向させて収容する。試験片１０と半導体ウェハ１２ａ、１２ｂとを容器２０内に収容した状態で、熱処理炉１４において加熱する。その後、熱処理された半導体ウェハ１２ａの特性を測定して、試験片による半導体ウェハの汚染の程度を評価する。



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【特許請求の範囲】

【請求項1】　半導体用治具に用いられる材料を評価する方法であって、

石英、炭化ケイ素、シリコンおよびそれらの組合せからなる群から選択される材料からなりかつ通気孔を有する容器内に、前記半導体用治具に用いられる材料からなる試験片と半導体ウェハとを、互いに接触させずにかつ互いの距離が２０ｍｍ以下となるよう対向させて収容する工程と、

前記試験片と前記半導体ウェハとを前記容器内に収容した状態で熱処理炉において加熱する工程と、

前記加熱工程の後、前記半導体ウェハの特性を測定する工程とを備え、

前記容器の通気孔のサイズは、前記加熱工程において前記熱処理炉および前記容器の外の雰囲気からの前記半導体ウェハの汚染を抑制しながら通気を行なうことができる程度の大きさであり、

前記半導体ウェハの特性を測定することにより前記半導体用治具に用いられる材料による半導体ウェハへの汚染性を評価することを特徴とする、半導体用治具材料の評価方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体用治具に用いられる材料を評価する方法に関し、特に、半導体装置の製造プロセスにおける熱処理工程に際し、該材料が半導体ウェハに対してどれほど汚染をもたらすかについて簡便かつ適切に評価するための方法に関する。

【０００２】

【従来の技術】半導体装置の製造プロセスに用いられるウェハボートやプロセスチューブ等の半導体用治具には、半導体熱処理工程等において有害な金属不純物による半導体ウェハの汚染を引起こさないものが望まれる。そのような半導体用治具を製造するため、治具に用いる材料の半導体ウェハに対する汚染性を正しく評価することが肝要である。従来、この評価方法として主に次の３つの方法が存在した。

【０００３】第１の方法は、治具材料を粉砕し酸等に溶解して得られる溶液中の金属不純物を原子吸光分析、誘導結合型プラズマ分析（ＩＣＰ）等で定量する方法である。

【０００４】第２の方法は、評価の対象となる治具材料でプロセスチューブやウェハボート等の半導体用治具を実際に作製し、得られた半導体用治具上で半導体ウェハを熱処理して、ウェハの汚染状況を評価する方法である。

【０００５】第３の方法は、金属不純物の拡散係数が半導体より小さい物質たとえば窒化ケイ素で被覆された金属捕集用物体を治具材料とともに熱処理し、金属捕集用物体の被覆内に捕集された金属不純物を定量する方法である（特開平４－２６７３２７号公報参照）。

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【０００６】第１の方法では、治具材料中に含まれる金属不純物の種類と量を明らかにすることができるが、金属不純物の形態（たとえば酸化物、炭化物等）および治具の使用条件（温度、雰囲気等）によって異なる実際の汚染度については明らかにすることができない。この方法では、実際の熱処理工程において治具材料が半導体特性にどれほどの影響を与えるかどうかを明確にすることはできない。

【０００７】第２の方法では、実際に対象となる治具をいちいち試作する必要がある。試験に用いられる熱処理設備も、治具の必要とするスペース等によって制約を受ける。この方法は、コスト、時間、便宜性の点で実際的ではない。

【０００８】第３の方法でも、第１の方法と同様に汚染物質の同定、定量が可能であるが、実際の熱処理工程における半導体特性への影響は明確にならない。この方法の一具体例として、窒化ケイ素等で被覆された金属捕集用物体を治具材料で挟んで熱処理し、被覆に捕集された金属不純物を分析し、治具材料の汚染性を評価する方法がある。しかし、この方法のように、治具材料と金属捕集用物体とを接触させて熱処理を行なうと、たとえば酸素誘因積層欠陥（Oxidation-Induced StackingFaults）（以下、「ＯＳＦ」と称する）を誘発し、正確な材料評価ができなくなる。またこの方法は、金属捕集用物体という特別な材料を必要とするため、コスト、評価時間の点にも問題がある。

【０００９】

【発明が解決しようとする課題】本発明の目的は、半導体ウェハへの汚染性に関し、半導体用治具に用いられる材料を簡便かつ的確に評価することのできる方法を提供することである。

【００１０】

【課題を解決するための手段】本発明は、半導体用治具に用いられる材料を評価する方法であって、石英、炭化ケイ素、シリコンおよびそれらの組合せからなる群から選択される材料からなりかつ通気孔を有する容器内に、半導体用治具に用いられる材料からなる試験片と半導体ウェハとを、互いに接触させずにかつ互いの距離が２０ｍｍ以下となるよう対向させて収容する工程と、試験片と半導体ウェハとを容器内に収容した状態で熱処理炉において加熱する工程と、加熱工程の後、半導体ウェハの特性を測定する工程とを備える。試験片および半導体ウェハを収容する容器の通気孔のサイズは、加熱工程において熱処理炉および該容器の外の雰囲気からの半導体ウェハの汚染を抑制しながら通気を行なうことができる程度の大きさである。試験片とともに加熱された半導体ウェハの特性を測定することにより半導体用治具に用いられる材料による半導体ウェハへの汚染性を評価することができる。

【００１１】試験片および半導体ウェハを収容する容器は、対向する１対の底面とそれらに挟まれた側面とにより試験片および半導体ウェハを収容するための空間を形成するものとすることができる。この場合、容器に設けられる通気孔における開口面積は、１対の底面のいずれかの面積の１／２０～１／１０とすることが好ましい。

【００１２】

【発明の実施の形態】本発明は、半導体装置製造プロセスに用いられるウェハボート、プロセスチューブ等の半導体用治具を構成する材料の評価に適用される。本発明は、簡便かつ的確な評価に適した形状および寸法の治具材料を用いて、試験設備の制約を少なくし、費用および時間の負担を軽くすることができるものである。たとえば、評価のために容器内に収容する治具材料の形状および寸法を、ともに容器内に収容される半導体ウェハとほぼ同じにすることはより実際的でかつより好ましい。

【００１３】本発明では、適当な形状および寸法に成形された治具用材料からなる試験片と半導体ウェハとを、石英、炭化ケイ素、シリコンおよびそれらの組合せからなる群から選択される材料からなる半密閉の容器内に収容する。この容器は、中に収容される試験片および半導体ウェハを、後の加熱工程において熱処理炉および加熱雰囲気の影響から保護する役割を果たす。また容器は、加熱工程において熱処理炉および容器の外の雰囲気からの半導体ウェハの汚染を抑制しながら通気を行なうことができる程度の大きさの隙間を有する。この隙間により、容器内雰囲気と容器外雰囲気との間の流通を徐々に行なって、容器自体および容器内雰囲気からの試験片および半導体ウェハへの影響を小さくすることができる。容器は、試験片および半導体ウェハを取囲んで保護し、半導体ウェハに対する試験片からの影響が他の要因からの影響に妨害されないよう、的確な評価のための環境をもたらす。容器は、加熱工程において試験片および半導体ウェハに汚染の影響を極力与えないものが望ましいため、その材料として石英、炭化ケイ素、シリコンまたはそれらの組合せが選択される。より好ましい材料として、石英ガラス、炭化ケイ素の焼結体、炭化ケイ素およびシリコンからなる炭化ケイ素質複合材料、シリコン、炭化ケイ素に炭化ケイ素をＣＶＤコートしたものおよび炭化ケイ素のＣＶＤコート膜で被覆された材料（たとえば炭素材）等がある。容器を構成する材料において、各金属不純物の濃度は、たとえば１ｐｐｍ以下が望ましい。容器は、全体を１種類の材料から構成してもよいし、異なる材料からなる部分で構成してもよい。また、特定の材料からなる基材上に他の材料をコーティングして容器を形成してもよい。

【００１４】容器内に収容された試験片および半導体ウェハは、熱処理炉において加熱される。図１は、本発明の一具体例を示すものであり、試験片と半導体ウェハとを容器内に収容した状態で熱処理炉において加熱する様子を示している。熱処理炉１４内には、治具用材料からなる試験片１０および半導体ウェハ１２ａ、１２ｂを収容する半密閉容器２０が載置されている。試験片１０は、半導体ウェハ１２ａおよび１２ｂとはぼ同じ形状および寸法とすることができる。それにより、半密閉容器２０の構造を簡単にすることができ、得られる評価のばらつきも減少させることができる。試験片１０を半導体ウェハ１２ａおよび１２ｂに対向させた状態で半密閉容器２０内に収容し、熱処理を行なう。熱処理においては、ヒータ１５により炉１４内の温度を所定の温度に上昇させ、必要な時間保持する。また、熱処理に際し半導体装置製造プロセスに用いられるO_2等の所定のガスを導入孔１６を介して炉１４内に導入し、所定の雰囲気がもたらされる。

【００１５】図１に示すように、半密閉容器２０は、試験片１０および半導体ウェハ１２ａ、１２ｂを収容する支持体２２と、それを覆う蓋体２１とから構成される。支持体２２には、試験片およびウェハを支持するための棚部が形成されており、試験片と半導体ウェハとを所定の距離で離した状態でほぼ平行に保持できるようになっている。支持体２２において、少なくとも１つの試験片および半導体ウェハを収容することができるよう少なくとも２つの棚部が形成されるが、その数は２以上で必要に応じて設定することができる。評価を行ないたい試験片の数に応じて適当な数の棚部を有する支持体を用いることができる。容器２０を構成する蓋体２１および支持体２２により、試験片および半導体ウェハは取囲まれた状態で収容されるが、支持体２２と蓋体２１との間には隙間２３が形成されており、容器の内部は隙間２３で構成される通気孔により容器外部とつながっている。隙間２３は、後述するように、熱処理炉そのものからの汚染の影響、導入ガスによる汚染の影響、および半密閉容器からの汚染の影響をできるだけ小さくするよう、適当な大きさとされる。

【００１６】図２および図３に、半密閉容器を構成する支持体および蓋体の一具体例について、より詳細な構造を示す。図２に示す支持体２２は、一端が開口である箱状の形体である。支持体２２の側壁は完全な筒体ではなく、一部が欠けている。側壁に凸状に形成された棚部２２ａ、２２ｂおよび２２ｃは試験片および半導体ウェハを支持するようになっている。図３に示す蓋体２１は、一方端が開口である箱状の形体であり、支持体２２を覆うことができるよう、支持体２２よりも若干大きく、これを支持体２２に被せた時に隙間ができるようになっている。図４は、隙間ができる様子を示している。支持体２２の棚部に試験片および半導体ウェハを載置し、蓋体２１を被せれば、熱処理に必要な状態ができあがる。

【００１７】図１に示すように、試験片１０と半導体ウェハ１２ａおよび１２ｂとは、互いに接触しないように容器２０内に収容される。対向して保持される試験片１

0と半導体ウェハ12aまたは12bとの間隔は20mm以下に設定され、好ましくは0．3mm～10mmの範囲に設定される。この間隔が20mmを超えると、半導体ウェハに関し、試験片からの影響に比べて容器内雰囲気からの影響が相対的に大きくなり、試験片の半導体ウェハに対する汚染性について正確な評価ができなくなる。なお、間隔が0．3mmを下回ると、試験片と半導体ウェハとが接触しやすくなる。これらが接触した場合、後述するように半導体ウェハに発生するOSFのために正確な評価ができなくなる。また、半密閉容器20の支持体22と試験片および半導体ウェハとの接触面積は、これらを安定して支持できる範囲において可能な限り小さくすることが好ましい。接触面積が大きくなると、特に半導体ウェハにおいて欠陥が生成しやすくなる。欠陥が多く生成すると、評価の正確さが損なわれるおそれがある。これらの接触面積を可能な限り小さくすることによって、より正確な評価を得ることができる。

【0018】半密閉容器20において、支持体22と蓋体21との隙間23は、加熱工程において熱処理炉および加熱雰囲気からの汚染の影響を抑制できるよう適当な大きさに設定される。図4は、支持体22に蓋体21を被せてなる半密閉容器20の断面を示すものである。支持体22と蓋体21との間には、隙間23が形成されている。隙間23は、容器の中と外をつなぐ通気孔を形成する。この通気孔の開口面積、すなわち隙間23の面積は、支持体22の底22eの面積の1／20～1／10の範囲にあることが好ましい。隙間の面積が底面積の1／20より小さいと、半密閉容器20内の雰囲気の影響が相対的に大きくなってくる。すなわち、半密閉容器内の雰囲気を試験目的の雰囲気に制御するのが困難になってくる。隙間の面積が底面積の1／10より大きいと、熱処理炉からの汚染および導入ガスからの汚染の影響が大きくなってくる。これらの影響が大きくなりすぎると、評価の正確さが損なわれるようになる。本発明は、適当なサイズの隙間を有する容器内に試験片と半導体ウェハとを収容し、上述した影響を極力避けて、治具材料の半導体ウェハに対する影響を確実に測定できる方法を提供するものである。

【0019】温度、時間および雰囲気等の熱処理条件は、半導体装置の製造プロセスにおいて治具が使用される条件に合わせるのが一般的である。しかしながら、必要に応じて熱処理時間を短縮したり、温度を上げて行なっても差し支えない。

【0020】熱処理の後、半導体ウェハの特性を測定することにより、試験片の半導体ウェハに対する影響、すなわち治具材料による半導体ウェハへの汚染性を評価することができる。半導体ウェハの特性を測定する方法には、シリコンウェハ等の材料評価に通常用いられている方法を適用することができる。半導体ウェハの特性を測定する方法として、ライフタイム測定法、OSF測定法、表面酸化膜分析法等を用いることができる。ライフタイム測定法は、マイクロ波減衰法とも呼ばれ、半導体ウェハを光等で励起したときに発生するキャリアの半減期を測定する方法である。重金属不純物の汚染により半減期は短くなるため、これを測定することによりウェハの汚染度の評価が比較的簡単にできる。ライフタイムが大きければ、試験片から半導体ウェハへの汚染の度合が小さく、したがって試験片は純度が高く治具により適したものであることを意味する。OSFは酸化処理中に発生する積層欠陥のことで、重金属や機械的傷により発生するものである。OSF測定法では、モニター用ウェハをエッチングして、OSFに起因するピット数を金属顕微鏡を用いて測定する。半導体ウェハにおいて測定されたOSFが少ない場合、試験片からウェハへの汚染の度合が小さく、したがって、治具材料は純度が高く、治具を構成するために望ましいことを意味する。表面酸化膜分析法は、酸化雰囲気中で酸化した際に半導体ウェハに生成する表面酸化膜中の不純物を定量し、汚染源を明確化するものである。この方法では、たとえば原子吸光分析により不純物を定量する。このようにして試験片とともに熱処理された半導体ウェハの特性を測定することにより、治具材料の半導体ウェハに対する汚染性を評価することができ、その材料が半導体用治具に適切なものであるかどうかを簡便かつ的確に把握することができる。

【0021】

【実施例】

実施例1

表1に示す純度をそれぞれ有する3種類の炭化ケイ素焼結体からなる半導体用治具材料A、BおよびCについて評価を行なった。半導体装置の製造に通常用いられる4インチシリコンウェハを材料評価のためのモニタ用ウェハとした。3種類の治具材料についてそれぞれ4インチシリコンウェハと同じ形状および寸法に調製したものを試験片として用いた。図2に示すような支持体と図3に示すような蓋体とからなる石英製の半密閉容器に、それぞれの治具材料からなる試験片とモニタウェハとを図1に示すようにして半密閉容器内に収容した。すなわち、各試験片を対向する2枚のモニタ用ウェハの間に載置した。モニタ用ウェハと治具材料試験片との間隔は、5mmであった。支持体に蓋体を被せたときにできる隙間の面積は、支持体の底面積の1／15であった。試験片およびモニタ用ウェハを半密閉容器内に収容した状態で、図1に示すように、熱処理炉において乾燥O2雰囲気下で1200℃、2時間の熱処理を行なった。

【0022】熱処理の後、モニタ用ウェハを取出し、ウェハの特性を測定した。通常の方法に従い、モニタ用ウェハの試験片に対向していた面のライフタイム（LT）、OSF個数、酸化膜中の金属不純物について測定を行なった。ライフタイムは、レオ技研社製LTA－33Aにより測定した。OSF個数は、前述のように金属

顕微鏡により測定した。酸化膜中の金属不純物は、フレームレス原子吸光分析により測定を行なった。測定の結果を表2に示す。ライフタイム、OSF個数、酸化膜中の金属不純物の測定値の間には矛盾がなく、これらにより各材料について精度のよい評価ができた。

【0023】図5は、材料Aの試験片とともに熱処理されたモニタ用ウェハ上のライフタイムの分布を示している。図6は、材料Bの試験片とともに加熱されたモニタ用ウェハ上のライフライムの分布を示している。図中には、書込まれた黒四角の大きさと半減期の長さとの関係をあわせて示している。図中の黒四角が大きいほどライフタイムが長いことを意味する。これらを比較すると、金属不純物の多い材料Bについてのモニタ用ウェハに関するライフタイムは短くなっていることがわかる。このことは、本発明が、材料の評価法として適正であることをさらに裏付けている。また注目すべきことは、表1に示す分析結果では、材料Aと材料Bの分析値はわずかに異なっているにすぎないのに対し、図5および図6に示すライフタイムの差は顕著なことである。すなわち、材料中の金属不純物を分析しただけでは、そのウェハに対する汚染性の優劣を的確に評価することは難しいことがわかる。

【0024】比較例1

各材料からなる試験片を2枚のモニタ用ウェハに挟んで密閉容器の同じ棚に載置した。すなわち、モニタ用ウェハと試験片とを互いに接触させて容器に収容した。それ以外は実施例1と同様の条件で処理を行ない、モニタ用ウェハの特性について測定を行なった。得られた結果を表2に示す。ライフタイムについては、実施例1と同様な結果が得られたが、OSF個数については材料Aと材料Bとに関する評価が逆転した。また、OSF個数についての材料Cに関する値は異常に大きかった。これらの結果は、モニタ用ウェハと試験片とを接触させることが評価方法において不適当であることを示している。

【0025】実施例2

炭化ケイ素焼結体からなる半密閉容器を用いた以外は、実施例1と同様の条件下で処理を行ない、モニタ用ウェハの特性について測定した。得られた結果を表2に示す。結果は実施例1と同様の傾向を示しており、本発明に従う評価方法が適正であることがわかった。

＊【0026】比較例2

評価対象である炭化ケイ素焼結体の各材料でシリコンウェハの熱処理に用いられるカセットボートを作製した。4インチシリコンウェハを作製したカセットボートに載置し、熱処理炉において乾燥O_2雰囲気中、1200℃、2時間の熱処理を行なった。図7は、シリコンウェハ7Zがカセットボート70上に載置されるようすを示している。このように実際にカセットボート上で熱処理を行なったシリコンウェハについて、実施例1と同様にライフタイム、OSF個数、酸化膜中の金属不純物を測定した。得られた結果を表2に示す。また、熱処理されたシリコンウェハにおけるライフタイムの分布を図8に示す。図8に示す分布では、ウェハにおいてカセットボートと接触している部分（図の下の部分）はライフタイムが異常に短くなっている。しかし、これは局部的な汚染によるものであり、ライフタイム値全体の平均値への影響は表2の結果が示すように比較的小さい。したがって、ライフタイムの平均値だけでウェハの汚染性を評価するのは危険であることがわかる。

【0027】比較例3

試験片とモニタ用ウェハの距離が25mmとなるような棚部が形成された支持体を半密閉容器に用いた以外は、実施例1と同様の条件で処理を行なった。材料Aの試験片を半密閉容器内でモニタ用ウェハとともに熱処理した後、実施例1と同様にウェハ上のライフライム分布を測定した。その結果を図9に示す。図に示すように、モニタ用ウェハの外周部近傍はライフタイムが異常に短くなっており、この部分は半密閉容器内部の雰囲気による汚染であると考えられた。したがって、試験片とモニタ用ウェハとの間の距離が大きすぎると正確な評価が困難になることがわかった。

【0028】

【表1】

特性 / 試料		基材純度(ppm)				
		Fe	Ni	Cu	Cr	Al
発明	材料A	<0.5	<1	<0.2	<0.5	2
〃	B	<0.5	<1	<0.2	<0.5	<1
〃	C	3	<1	<0.2	<0.5	<1

Tr：0.01ppm以下

【0029】

【表2】

特性 / 試料		LT (μS)	OSF (個/cm²)	酸化膜(×10¹²atom/cm³) Fe	Ni	Cu	Zn	Al
実施例1	材料A	356	2	2.0	<3.6	5.1	0.4	<2.2
〃	B	72	15	21	<3.6	4.4	0.4	<2.2
〃	C	6.1	80	105	195	5.2	4.1	<2.2
比較例1	材料A	323	25	2.3	<3.6	5.8	2.1	<2.2
〃	B	57	12	23	<3.6	3.5	0.7	<2.2
〃	C	4.6	2000	111	242	6.4	2.8	<2.2
実施例2	材料A	347	6	2.2	<3.6	3.5	0.5	<2.2
〃	B	68	24	25	<3.6	5.3	1.1	<2.2
〃	C	4.9	103	102	120	7.9	5.7	<2.2
比較例2	材料A	540	1	<1.2	<3.6	4.5	0.6	<2.2
〃	B	412	5	<1.2	<3.6	5.1	0.9	<2.2
〃	C	306	20	2.0	59	6.7	0.5	<2.2

【0030】

【発明の効果】以上のように本発明によれば、高温熱処理中に治具材料から放出される金属不純物を容易かつ高感度に検出することができるとともに、治具材料の半導体特性への影響を明確にすることができる。上述したように、本発明によれば、治具材料中の不純物がウェハ特性に与える影響を精度よく評価することができる。本発明は、従来の方法に用いられるような特殊な金属捕集材や治具自体を必要とせず、より多くの種類の治具材料について簡便かつ迅速に評価を行なうことができる。この点において、本発明はコスト、時間の点で従来法よりも優れている。本発明により治具材料を評価し、より適切な材料を見い出して治具を製造すれば、半導体装置の製造歩留りおよび信頼性の向上に大きく寄与する半導体用治具を提供することができる。

【図面の簡単な説明】

【図1】本発明に従って試験片および半導体ウェハを容器内に収容し、熱処理を行なう一具体例を示す模式図である。

【図2】本発明に用いられる容器の構成部分の一具体例を示す斜視図である。

【図3】本発明に用いられる容器の構成部分の一具体例を示す斜視図である。

【図4】図2に示す構成部分に図3に示す構成部分を被せることによりできる隙間を示す断面図である。

【図5】実施例1で得られたモニタ用ウェハにおけるライフタイムの分布を示す模式図である。

【図6】実施例1で得られたもう1つのモニタ用ウェハにおけるライフタイムの分布を示す模式図である。

【図7】比較例2においてウェハをカセットボートに載置した状態を示す模式図である。

【図8】比較例2において得られたモニタ用ウェハにおけるライフタイムの分布を示す模式図である。

【図9】比較例3で得られたモニタ用ウェハにおけるライフタイムの分布を示す模式図である。

【符号の説明】

10　試験片

12a、12b　半導体ウェハ

14　熱処理炉

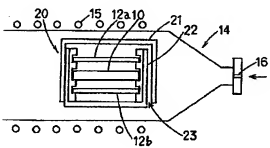
20　半密閉容器

21　蓋体

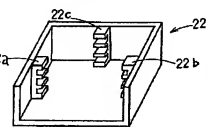
22　支持体

23　隙間

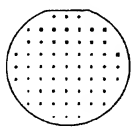
【図1】



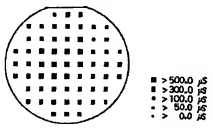
【図2】



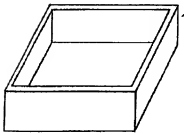
【図6】



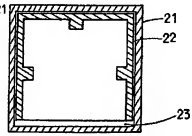
【図5】



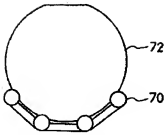
【図3】



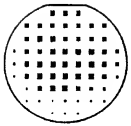
【図4】



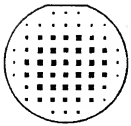
【図7】



【図8】



【図9】



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(51)Int.Cl.[6]	識別記号	FI
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